BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

As rescanning documents *will not* correct images, please do not report the images to the Image Problem Mailbox.

REMARKS

Applicant amends claims 26-28 and 33-40 to better define the subject matter of the invention. Attached hereto is a marked-up version of the changes made to the claims by the current amendment.

Claims 26 and 27 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. patent 5,358,901 (Fiordalice et al.).

Claim 26, as amended, defines a semiconductor device and recites, in part, "a via hole" and "a first titanium aluminide layer lining at least a bottom of the via hole" and "a second titanium aluminide layer or a titanium layer on sides of said via hole." This claimed device is not anticipated by Fiordalice et al.

Fiordalice et al. at column 3, lines 62-66, inter alia, forecloses the possibility of anticipating the claimed device in stating, "the titanium aluminide layer 61 is formed only along the bottom of the via opening 52 and does not contact the ILD layer 51 except near the bottom of the via opening 52" and "no unreacted titanium is formed on the ILD layer 51." The requirements set forth in the preceeding excerpts from Fiordalice et al. are reinforced at column 4, line 44 to column 5, line 32, where the reference sets forth the reasoning for having no titanium aluminide or unreated titanium on the sides of the via opening (52).

Since Fiordalice et al. does not disclose each recited element of the device of claim 26, the claim is not anticipated. Applicant respectfully requests that the 35 U.S.C. § 102(b) rejection of claim 26 be withdrawn.

Claim 27, as amended, defines a semiconductor device and recites, in part, "a via hole" and "a titanium aluminide layer lining a bottom and sides of the via hole." For the same reasoning set forth relating to the patentability of claim 26 over Fiordalice et al., claim 27 is

likewise not anticipated because Fiordalice et al. forecloses the possibility of a titanium aluminide layer lining any part of a via opening other than the bottom (column 3, lines 62-65). Applicant respectfully requests that the 35 U.S.C. § 102(b) rejection of claim 27 be withdrawn.

Claims 28-33 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Fiordalice et al. in view of U.S. patent 5,313,101 (Harada et al.) and further in view of U.S. patent 5,281,850 (Kanamori). Applicant respectfully traverses this rejection.

Claim 28, as amended, defines a semiconductor memory device and recites, in part, "a via hole" and "a first titanium aluminide layer lining at least a bottom of the via hole" and "a second titanium aluminide layer or a titanium layer on sides of said via hole" and "a titanium compound containing layer on the first titanium aluminide layer and in contact with said first titanium aluminide layer at an interface that is substantially free of tensile stress." This device is not taught or suggested by the combination of Fiordalice et al., Harada et al., and Kanamori. In fact, such combination is improper since Fiordalice et al. teaches away from recited limitations of the claim as well as from combination with other references for rendering the claimed subject matter obvious.

In considering any patent as a reference for 35 U.S.C. § 103 purposes, it must be considered as a whole, including any teaching away, and further, it must suggest the desirability and obviousness of combining it with the other references. M.P.E.P. §§ 2141.01 and 2141.02 (2001) (emphasis added). In accordance with M.P.E.P. § 2144.05.III, a prima facie case of obviousness is rebutted by showing that a reference, in any material respect, teaches away from the claimed invention. M.P.E.P. § 2144.05.III (2001) (emphasis added), citing In re Geisler, 116 F.3d 1465, 1471, 43 U.S.P.Q.2d 1362, 1366 (Fed. Cir. 1997). "A prior art reference that 'teaches away' from the claimed invention is a significant factor to be considered in determining obvious." M.P.E.P. § 2145.X.*D*.1 (2001). "References cannot be

combined where [a] reference teaches away from their combination" for the purposes of supporting a rejection under 35 U.S.C. § 103(a). Id. at X.*D*.2. Fiordalice et al. does not teach or suggest the claimed method and, in fact, teaches away from the claimed method and from its combination with Harada et al. and is, therefore, an improper reference for use in rejecting the claims under 35 U.S.C. § 103(a).

As discussed above regarding the anticipation rejection of claims 26 and 27, Fiordalice et al. does not anticipate a device such as claimed since, according to its disclosure, the via disclosed therein cannot have titanium aluminide or titanium on its sides (column 3, lines 62-66). Thus, Fiordalice et al. teaches away from the claimed invention. Also, Fiordalice et al. cannot be combined with Harada et al. or Kanamori for the same reasoning because the portions of the devices disclosed by Fiordalice et al. and Harada et al. are incompatible as Fiordalice et al. does not allow any titanium aluminide or titanium on the sides of its disclosed via and the device of Harada et al. (FIG. 2G) is disclosed as requiring the opposite structure. Thus, these references could not have been combined to have rendered the subject matter of claim 26 obvious.

Even if Fiordalice et al. was not improperly combined with the other cited references, it does not teach or suggest the claimed invention since the via disclosed therein does not have a layer of titanium aluminide or titanium on its sides. Neither Harada et al. nor Kanamori, individually or combined with one another, teaches or suggests the claimed invention either.

Since the combination of Fiordalice et al., Harada et al., and Kanamori is improper, and even if it were not, would not have taught or suggested the claimed invention, independent claim 28 is patentable over these references. Likewise, dependent claims 29-32 are patentable at least because they incorporate all the limitations of claim 28. Applicant respectfully requests that the 35 U.S.C. § 103(a) rejection of claims 28-32 be withdrawn.

Claim 33, as amended, defines a memory module including a random access memory and recites, in part, "a via hole" and "a titanium aluminide layer lining at least a bottom of the via hole" and "a titanium layer lining sides of the via hole" and a "titanium compound layer being in contact with said titanium aluminide layer, wherein said titanium compound layer experiences approximately no tensile stress from said titanium aluminide layer." The combination of Fiordalice et al., Harada et al., and Kanamori, even if not improper, would not have taught or suggested the claimed device.

Fiordalice et al. teaches away from the subject matter of claim 33 for similar reasoning to that set forth above relating to the patentability of claim 28. Fiordalice et al. expressly forecloses the possibility of having any titanium on the sides of its disclosed via opening (52) in the ILD layer (51). Thus, Fiordalice et al. teaches away from the claimed invention, and further, does not teach or suggest the claimed invention. Also, Fiordalice et al. teaches away from combination with Harada et al. for the same reasoning set forth above relating to the patentability of claim 28.

Harada et al. and Kanamori cannot teach or suggest the recited elements of the device of claim 33 by themselves and would not have individually, or in combination with each other, rendered the claimed subject matter obvious.

Since the combination of Fiordalice et al., Harada et al., and Kanamori is improper, and even if it were not, would not have taught or suggested the claimed invention, claim 33 is patentable over these references. Applicant respectfully requests that the 35 U.S.C. § 103(a) rejection of claim 33 be withdrawn.

Claims 34-40 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Fiordalice et al. in view of U.S. patent Harada et al. and further in view of U.S. patent 4,656,605 (Clayton). Applicant respectfully traverses this rejection.

Claim 34, as amended, defines a memory module including a random access memory and recites, in part, "a via hole" and "a first titanium aluminide layer lining at least a bottom of the via hole" and "a second titanium aluminide layer or a titanium layer lining sides of the via hole" and "a conductive material on the first titanium aluminide layer, wherein said conductive material and said first titanium aluminide layer are in contact at an interface having approximately no tensile stress from said first titanium aluminide layer." The impropriety of the combination of Fiordalice et al. with other reference to reject the claims for obviousness, as well as its teaching away from the claimed device (particularly the second titanium aluminide or titanium layer recited), has been discussed at length above. Additionally, neither Harada et al. nor Clayton, individually or in combination teaches or suggests the claimed subject matter. Applicant respectfully requests that the 35 U.S.C. § 103(a) rejection of claim 34 be withdrawn.

Claim 35, as amended, defines a memory module including a random access memory and recites, in part, "a via hole" and "a titanium aluminide layer lining a bottom of the via hole" and "a titanium layer lining sides of the via hole" and "a titanium nitride layer is in contact with said titanium aluminide layer at an interface, said interface being substantially free of tensile stress between said titanium aluminide layer and said titanium nitride layer." As already discussed at length relating to the patentability of claims 26-33, Fiordalice et al. teaches away from a titanium layer lining the sides of a via hole, as claimed. Also, as already discussed, Fiordalice et al. is not properly combined with Harada et al. and Clayton. Neither Harada et al. nor Clayton, individually or combined, can teach or suggest the claimed device. Applicant respectfully requests that the 35 U.S.C. § 103(a) rejection of claim 35 be withdrawn.

Claim 36, as amended, defines a memory module including a random access memory and recites, in part, "a first metallic layer over the first dielectric layer, said first metallic layer comprising aluminum" and "a via hole extending through the second dielectric

layer to a surface of the first metallic layer" and "a titanium aluminide layer lining a bottom of the vial hole" and "a conductive plug material on the titanium aluminide layer, said conductive plug material comprising aluminum." This device is not taught or suggested by Fiordalice et al., Harada et al., and Clayton, taken individually or in combination, even if such combination was not improper.

None of Fiordalice et al., Harada et al., or Clayton, individually or in combination teaches or suggests a via to an aluminum containing layer, a titanium aluminide layer over that aluminum-containing layer in the via, and an aluminum-containing plug in the via on the titanium aluminide layer. Such a device, or portion thereof, is simply not disclosed in any of the references. No combination of the cited references can teach or suggest the necessary elements to disclose the claimed device or render it obvious.

Since the subject matter of claim 36 would not have been obvious over the cited references, it is patentable thereover. Applicant respectfully requests that the 35 U.S.C. § 103(a) rejection of claim 36 be withdrawn.

Claim 37, as amended, defines a computer system including a semiconductor chip and recites, in part, "a via hole" and "a titanium aluminide layer lining a bottom and sides of the via hole." Since Fiordalice et al. teaches away from the claimed device and cannot be properly combined with Harada et al. and Clayton, and since neither Harada et al. nor Clayton, taken individually or combined, teaches or suggests the claimed invention, the subject matter of claim 37 would not have been obvious over the cited references. Applicant respectfully requests that the 35 U.S.C. § 103(a) rejection of claim 37 be withdrawn.

Claim 38, as amended, defines a computer system including a computer chip and recites, in part, "a via hole" and "a first titanium aluminide layer lining at least a bottom of the via hole" and "a second titanium aluminide layer or a titanium layer lining sides of the via hole" and "a conductive material on the first titanium aluminide layer, wherein said conductive

material is in contact with said first titanium aluminide layer at an interface, said interface being substantially free of tensile stress between said first titanium aluminide layer and said conductive material." Since Fiordalice et al. teaches away from this claimed device and cannot be properly combined with Harada et al. and Clayton, and since neither Harada et al. nor Clayton, taken individually or combined, teaches or suggests the claimed invention, the subject matter of claim 38 would not have been obvious over the cited references. Applicant respectfully requests that the 35 U.S.C. § 103(a) rejection of claim 38 be withdrawn.

Claim 39, as amended, defines a computer system including a semiconductor chip and recites, in part, "a via hole" and "a titanium aluminide layer lining a bottom of the via hole" and a titanium layer lining sides of the via hole" and "a titanium nitride layer substantially free of through cracks on the titanium aluminide layer and the titanium layer, wherein said titanium nitride layer is in contact with said titanium aluminide layer and said titanium aluminide layer exerts approximately zero tensile stress upon said titanium nitride layer." Since Fiordalice et al. teaches away from this claimed device and also cannot be properly combined with Harada et al. and Clayton, and since neither Harada et al. nor Clayton, taken individually or combined, teaches or suggests the claimed invention, the subject matter of claim 39 would not have been obvious over the cited references. Applicant respectfully requests that the 35 U.S.C. § 103(a) rejection of claim 39 be withdrawn.

Claim 40, as amended, defines a computer system including a semiconductor chip and recites in part a "metallic layer comprising aluminum" and "a via hole extending through the second dielectric layer and the antireflective coating to a surface of the second metallic layer" and "a titanium aluminide layer lining a bottom of the via hole" and "a titanium layer lining sides of the via hole" and "a conductive plug material on the titanium aluminide layer, said conductive plug material comprising aluminum" and "a second metallic layer on the second dielectric layer and electrically connected to the plug material, said second metallic layer comprising aluminum." Since Fiordalice et al. teaches away from this claimed device and

cannot be properly combined with Harada et al. and Clayton, and since neither Harada et al. nor Clayton, taken individually or combined, teaches or suggests the claimed invention, the subject matter of claim 40 would not have been obvious over the cited references. Additionally, claim 40 is patentable for the same reasoning set for the above relating to the patentability of claim 36. Applicant respectfully requests that the 35 U.S.C. § 103(a) rejection of claim 40 be withdrawn.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

Dated: October 17, 2002

Respectfully submitted,

By_____

Thomas J. D'Amico
Registration No.: 28,371
Ryan H. Flax
Registration No.: 48,141
DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
2101 L Street NW
Washington, DC 20037-1526
(202) 785-9700
Attorneys for Applicant

Version With Markings to Show Changes Made

26. (Four Times Amended) A semiconductor device, comprising:

a metallic layer over a substrate;

a dielectric layer over said metallic layer;

a via hole extending through the dielectric layer to a surface of the metallic layer;

a first titanium aluminide layer lining at least a bottom of the via hole; [and]

a second titanium aluminide layer or a titanium layer on sides of said via hole; and

a conductive material on the first titanium aluminide layer, said conductive material and said first titanium aluminide layer being in contact at an interface, said interface being substantially free from tensile stress between said first titanium aluminide layer and said conductive material.

27. (Four Times Amended) A semiconductor device, comprising:

an aluminum layer over a substrate;

a dielectric layer over the aluminum layer;

a via hole extending through the dielectric layer to a surface of the aluminum layer;

a titanium aluminide layer lining [at least] a bottom and sides of the via hole;

a titanium nitride layer [substantially free of through cracks on] over the titanium aluminide layer[, wherein said titanium nitride layer is in contact with said titanium aluminide layer at an interface that is substantially free of tensile stress between said titanium aluminide layer and said titanium nitride layer]; and

a conductive plug material on the titanium nitride layer [; and

a metallic layer on the dielectric layer and electrically connected to the plug material].

28. (Four Times Amended) A semiconductor memory device, comprising:

a memory circuit region in a semiconductor substrate;

a first dielectric layer over the memory circuit region;

a first metallic layer over the first dielectric layer;

a contact interconnect between the first metallic layer and the substrate;

an antireflective coating over said first metallic layer;

a second dielectric layer [on] over the [first metallic layer] antireflective coating;

[an antireflective coating over said second dielectric layer;]

a via hole extending through the second dielectric layer and the antireflective coating to a surface of the [second] first metallic layer;

a first titanium aluminide layer lining at least a bottom of the via hole;

a second titanium aluminide layer or a titanium layer on sides of said via hole;

a titanium compound containing layer on the first titanium aluminide layer and in contact with said first titanium aluminide layer at an interface that is substantially free of tensile stress;

a conductive plug material on the titanium compound layer; and

a second metallic layer on the second dielectric layer and electrically connected to the plug material.

33. (Four Times Amended) A memory module, comprising:

a substrate comprising a circuit board;

a plurality of memory chips mounted on the substrate and connected to form a memory circuit, wherein one or more of the memory chips comprise a random access memory (RAM) fabricated on a semiconductor substrate comprising:

a first metallic layer over a substrate;

an antireflective coating over the first metallic layer;

a dielectric layer [on] over the [first metallic layer] antireflective coating;

[an antireflective coating over the dielectric layer;]

a via hole extending through the dielectric layer and the antireflective coating to a surface of the first metallic layer;

a titanium aluminide layer lining at least a bottom of the via hole;

a titanium layer lining sides of the via hole;

a titanium compound containing layer [on] over the titanium aluminide layer and the titanium layer, said titanium compound layer being in contact with said titanium aluminide layer, wherein said titanium compound layer experiences approximately no tensile stress from said titanium aluminide layer;

a conductive plug material formed [on] over the titanium compound layer; [and]

a second metallic layer on the dielectric layer and electrically connected to the plug material; and

[an edge] a connector [along one edge of] on the substrate [which is] and wired to said memory circuit.

34. (Four Times Amended) A memory module, comprising:

a substrate comprising a circuit board;

a plurality of memory chips mounted on the substrate and connected to form a memory circuit, wherein one or more of the memory chips comprise a random access memory (RAM) fabricated on a semiconductor substrate comprising:

a metallic layer over a substrate;

a dielectric layer over the metallic layer;

a via hole extending through the dielectric layer to a surface of the metallic layer;

a first titanium aluminide layer lining at least a bottom of the via hole; [and]

a second titanium aluminide layer or a titanium layer lining sides of the via hole; and

a conductive material on the first titanium aluminide layer, wherein said conductive material and said first titanium aluminide layer are in contact at an interface having approximately no tensile stress from said first titanium aluminide layer; and

[an edge] a connector [along one edge of] on the substrate [which is] and wired to said memory circuit.

35. (Four Times Amended) A memory module, comprising:

a substrate comprising a circuit board;

a plurality of memory chips mounted on the substrate and connected to form a memory circuit, wherein one or more of the memory chips comprise a random access memory (RAM) fabricated on a semiconductor substrate comprising:

an aluminum layer over a substrate;

a dielectric layer over the aluminum layer;

a via hole extending through the dielectric layer to a surface of the aluminum layer;

a titanium aluminide layer lining [at least] a bottom of the via hole;

a titanium layer lining sides of the via hole;

a titanium nitride layer substantially free of through cracks on the titanium aluminide layer, wherein said titanium nitride layer is in contact with said titanium aluminide layer at an interface, said interface being substantially free of tensile stress between said titanium aluminide layer and said titanium nitride layer;

a conductive plug material on the titanium nitride layer; and

a metallic layer on the dielectric layer and electrically connected to the plug material; and

[an edge] a connector [along one edge of] on the substrate [which is] and wired to said memory circuit.

36. (Four Times Amended) A memory module, comprising:

a substrate comprising a circuit board;

a plurality of memory chips mounted on the substrate and connected to form a memory circuit, wherein one or more of the memory chips comprise a random access memory (RAM) fabricated on a semiconductor substrate comprising:

a memory circuit region in a semiconductor substrate;

a first dielectric layer over the memory circuit region;

a first metallic layer over the first dielectric layer, said first metallic layer comprising aluminum;

a contact interconnect between the first metallic layer and the substrate;

a second dielectric layer over the first metallic layer;

a via hole extending through the second dielectric layer to a surface of the [second] first metallic layer;

a titanium aluminide layer lining [at least] a bottom of the via hole;

[a titanium compound layer on the titanium aluminide layer at a contact interface, wherein said contact interface experiences approximately no tensile stress from said titanium aluminide layer;]

a conductive plug material on the titanium [compound] aluminide layer, said conductive plug material comprising aluminum; and

a second metallic layer on the second dielectric layer and electrically connected to the plug material; and

[an edge] a connector [along one edge of] on the substrate [which is], said connector being wired to said memory circuit.

37. (Four Times Amended) A computer system, comprising:

a processor; and

a random access memory (RAM) fabricated on a semiconductor chip communicating with the processor and comprising:

a first metallic layer over a substrate;

a dielectric layer over the first metallic layer;

a via hole extending through the dielectric layer to a surface of the first metallic layer;

a titanium aluminide layer lining [at least] a bottom and sides of the via hole;

a titanium compound containing layer [on] over the titanium aluminide layer [, wherein said titanium compound layer is in contact with said titanium aluminide layer at an interface, said interface being substantially free of tensile stress between said titanium aluminide layer and said titanium compound layer] ;

a conductive plug material formed on the titanium compound layer; and

a second metallic layer [on] over the dielectric layer and electrically connected to the plug material.

38. (Four Times Amended) A computer system, comprising:

a processor; and

a random access memory (RAM) fabricated on a semiconductor chip communicating with the processor and comprising:

a metallic layer over a substrate;

an antireflective coating over the metallic layer;

a dielectric layer over the [metallic layer] antireflective coating;

[an antireflective coating over the dielectric layer;]

a via hole extending through the dielectric layer and the antireflective coating to a surface of the metallic layer;

a first titanium aluminide layer lining at least a bottom of the via hole; [and]

a second titanium aluminide layer or a titanium layer lining sides of the via hole; and

a conductive material on the first titanium aluminide [liner] layer, wherein said conductive material is in contact with said first titanium aluminide layer at an interface, said interface being substantially free of tensile stress between said first titanium aluminide layer and said conductive material.

39. (Four Times Amended) A computer system, comprising:

a processor; and

a random access memory (RAM) fabricated on a semiconductor chip communicating with the processor and comprising:

an aluminum layer over a substrate;

a dielectric layer over the aluminum layer;

a via hole extending through the dielectric layer to a surface of the aluminum layer;

a titanium aluminide layer lining [at least] a bottom of the via hole;

a titanium layer lining sides of the via hole;

a titanium nitride layer substantially free of through cracks on the titanium aluminide layer and the titanium layer, wherein said titanium nitride layer is in contact with said titanium aluminide layer and said titanium aluminide layer exerts approximately zero tensile stress upon said titanium nitride layer;

a conductive plug material on the titanium nitride layer; and

a metallic layer on the dielectric layer and electrically connected to the plug material.

40. (Four Times Amended) A computer system, comprising:

a processor; and

a random access memory (RAM) fabricated on a semiconductor chip communicating with the processor and comprising:

a memory circuit region in a semiconductor substrate;

a first dielectric layer over the memory circuit region;

a first metallic layer over the first dielectric layer, said metallic layer comprising aluminum;

a contact interconnect between the first metallic layer and the substrate;

an antireflective coating over the first metallic layer;

a second dielectric layer over the [first metallic layer] antireflective coating;

[an antireflective coating over the second dielectric layer;]

a via hole extending through the second dielectric layer and the antireflective coating to a surface of the second metallic layer;

a titanium aluminide layer lining [at least] a bottom and sides of the via hole;

[a titanium compound layer on the titanium aluminide layer, wherein said titanium compound layer is in contact with said titanium aluminide layer at an interface, said interface being substantially free of tensile stress between said titanium aluminide layer and said titanium compound layer;]

a conductive plug material on the titanium [compound] aluminide layer, said conductive plug material comprising aluminum; and

a second metallic layer on the second dielectric layer and electrically connected to the plug material, said second metallic layer comprising aluminum.